

=> dis his

(FILE 'HOME' ENTERED AT 14:44:56 ON 15 OCT 2001)

FILE 'USPATFULL' ENTERED AT 14:45:05 ON 15 OCT 2001

L1 199788 S (VARIABLE OR DIFFERENT OR MULTIPLE) (3A) (SIZE# OR LENGTH#)  
L2 22146 S CACHE#  
L3 898 S CACHE# ENTRY  
L4 9 S L1 (P) L3  
L5 2253 S CACHE (2A) (ENTR### OR SEGMENT#)  
L6 672 S L5 AND L1  
L7 51 S L5 (P) L1  
L8 46 S (INTERNAL OR EXTERNAL) (3A) (TRANSACTION? (2A) (BUFFER# OR  
RE  
L9 4850 S CACHE# (3A) (MISS? OR HIT#)  
L10 14 S L8 AND L9  
L11 10357 S MULTIPROCESS? OR (MULTI (W) PROCESS?)  
L12 37926 S PLURALITY (3A) PROCESS?  
L13 44029 S L11 OR L12  
L14 9 S L13 AND L10  
L15 1 S L1 AND L14

=> dis l14 1- pn,ti

YOU HAVE REQUESTED DATA FROM 9 ANSWERS - CONTINUE? Y/(N):y

L14 ANSWER 1 OF 9 USPATFULL

PI US 6195748 B1 20010227

TI Apparatus for sampling instruction execution information in a processor pipeline

L14 ANSWER 2 OF 9 USPATFULL

PI US 6108735 20000822

TI Method and apparatus for responding to unclaimed bus transactions

L14 ANSWER 3 OF 9 USPATFULL

PI US 5903738 19990511

TI Method and apparatus for performing bus transactions in a computer system

L14 ANSWER 4 OF 9 USPATFULL

PI US 5721855 19980224

TI Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer

L14 ANSWER 5 OF 9 USPATFULL

PI US 5696910 19971209

TI Method and apparatus for tracking transactions in a pipelined bus

L14 ANSWER 6 OF 9 USPATFULL

PI US 5682516 19971028

TI Computer system that maintains system wide cache coherency during deferred communication transactions

L14 ANSWER 7 OF 9 USPATFULL

PI US 5642494 19970624

TI Cache memory with reduced request-blocking

L14 ANSWER 8 OF 9 USPATFULL

PI US 5568620 19961022

TI Method and apparatus for performing bus transactions in a computer system

L14 ANSWER 9 OF 9 USPATFULL

PI US 5550988 19960827

TI Apparatus and method for performing error correction in a multi-processor system